ADC system with on-board demodulation for QUIET-II experiment

K. Ishidoshiro (KEK)

N. Makoto, T. Higuchi, M. Ikeno, M. Hasegawa, M. Hazumi, M.Tanaka, O. Tajima, T. Uchida

QUIET (Q/U imaging ExperimenT)

Experiment to hunt CMB B-modes induced by inflationary gravitational waves

One of the world best polarimeter array using HEMT amplifier technology

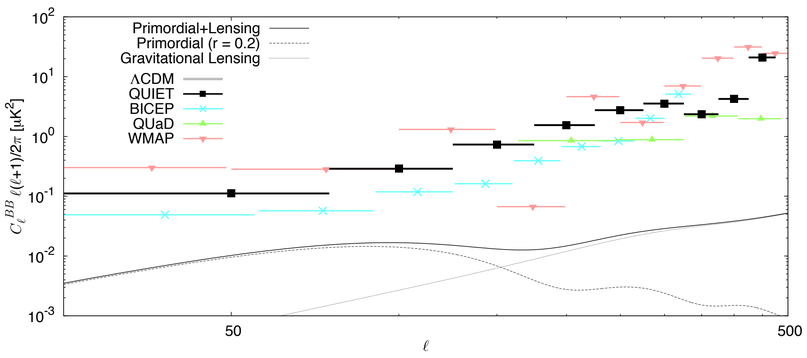
- W-band (90 GHz): 90 element, ~84uK√s
- Q-band (40 GHz): 19 element, ~70uK√s
- Strong immunity to systematic errors

Site: Chile, Chajnantor plateau

- 5080 m above sea level, Extremely low moisture

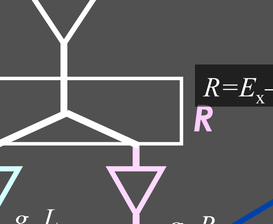
QUIET-I (2008 Oct. - 2010 Dec.)

- Q-band result: one of the stringent upper limit on B-mode spectrum
- W-band analysis: on going

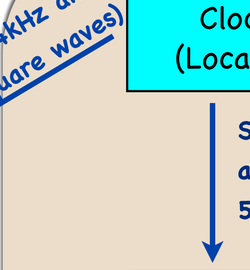


QUIET-II (proposed)

Scale up (90-element array -> 500-element array) using improved modules



Phase-I 90-element array



Phase-II 500-element array

ADC system for QUIET-II

Handle a large number of analog signals from polarimeters

(500-elements x 4ch = **2,000 signals**) on **the telescope mount**.

↔ limited space

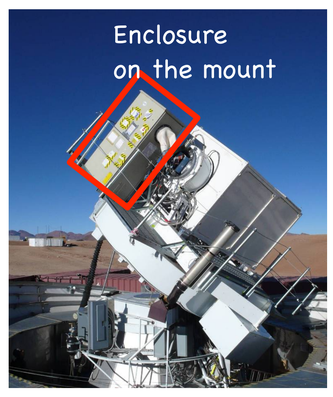
→ Compact and scalable system

No trigger and event concept

→ Record all time-ordered data (~100GB/day)

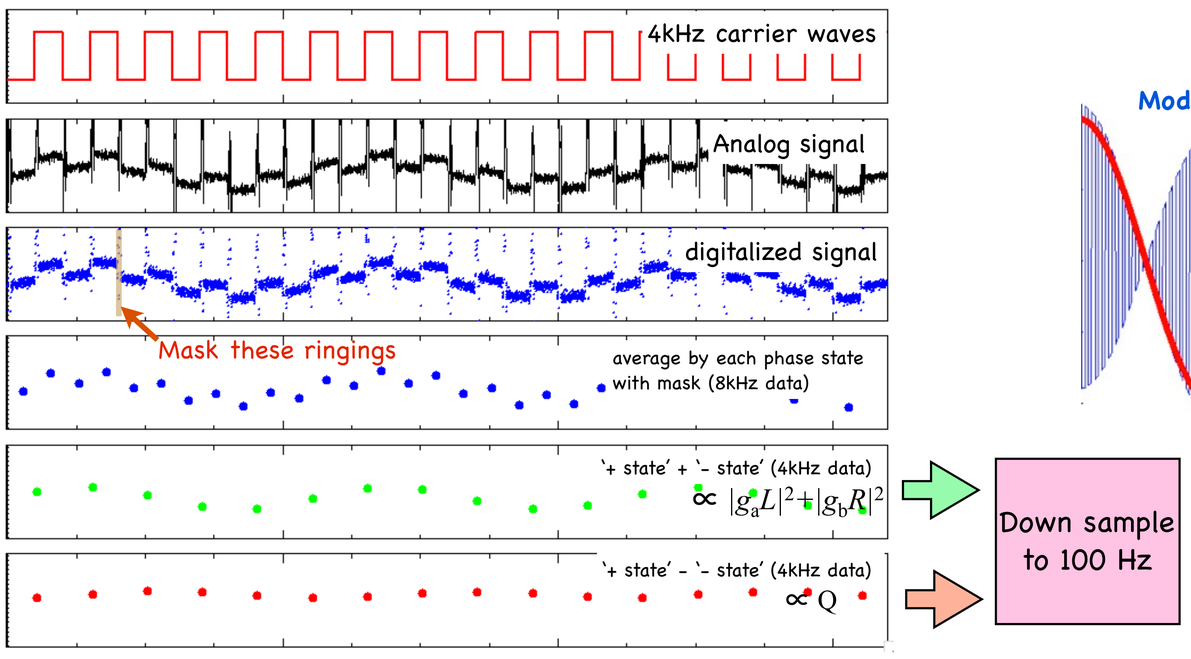
On-board demodulation

→ 1/f noise suppression



Polarimeters ADC system

Example of demodulation (in case of single 4kHz modulation)



Requirement for QUIET-II ADC system

Compact and scalable electronics, Easy data transfer

Digitalization with 800kHz sampling and 18 bits resolution

On-board demodulation and downsampling

Noise level: < 0.1uV/√Hz (ten times smaller than that of polarimeters)

Cross talk level: < -100 dB (immunity from fake polarization at the Phase-II level)

System components

ADC board

- # of ADC: 64
- VME6U-size

(VME crate used for only +5V power supply)

Nominal power: ~15 W

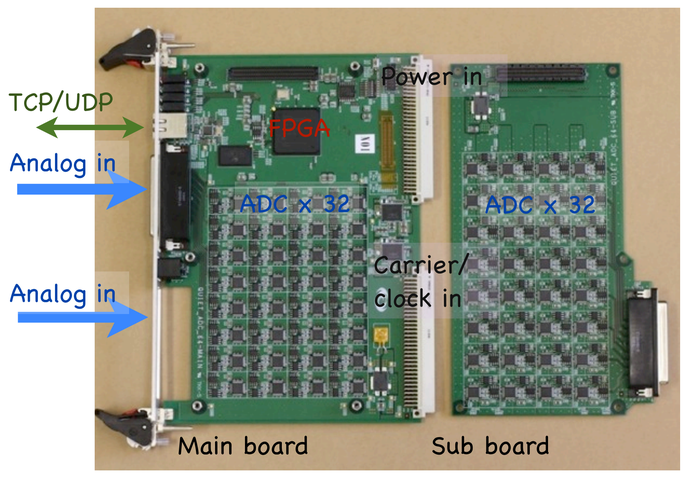
Same analog I/F with Phase-I ADC

- Differential input
- Dynamical range: +/- 1V
- Dsub78 connector

Demodulation/downsampling on FPGA

Hardware TCP/UDP processor (SiTCP)

- TCP for data transfer
- UDP for slow control



Clock master (Local oscillator)

2U-size

Distribution to 21 ADC boards

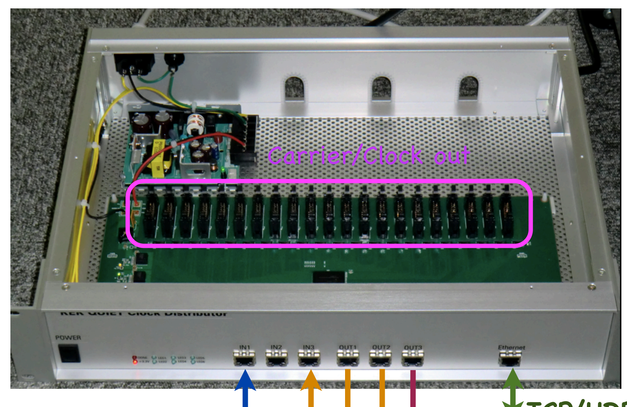
- Signal level: LVDS
- Cable: Flat cable
- System Clock: 40MHz
- Carriers: 4kHz, 50Hz

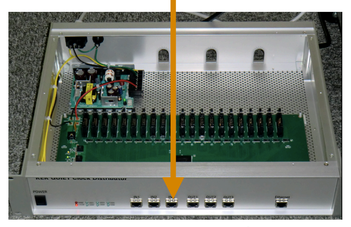
Hardware TCP/UDP processor (SiTCP)

- TCP for data transfer
- UDP for slow control

Synchronism using the front LVDS in/out

- Signal level: LVDS
- Cable: RJ45
- In: GPS, distributed system clock
- Out: Distributed system clock x2, carriers to polarimeters

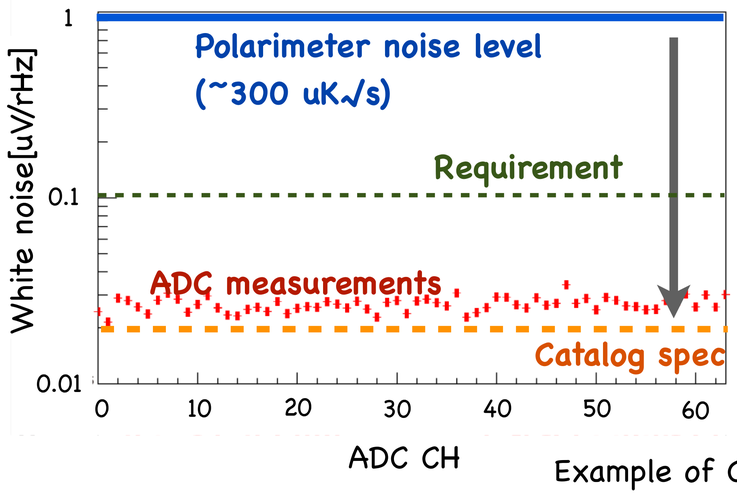




Other clock master (clock slave)

Prototype tests (single ADC board)

White noise measurement



1/30 - 1/50 of white noise of polarimeters

Typical noise level: 0.03 uV/√Hz

Cross talk measurement

Injection 1 Hz sine waves

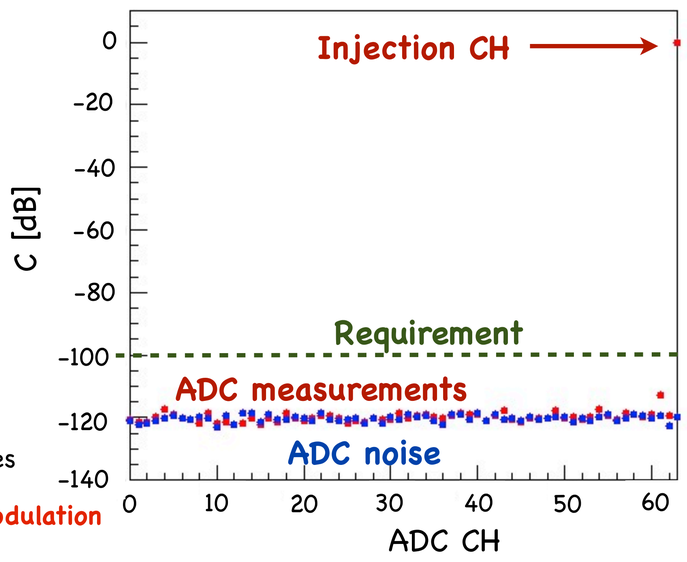
Typical time scale of CMB temperature 0.5 - 1 HZ

Comparison demodulated signal

$$C = \frac{\text{Demod. rms (CH i)}}{\text{Demod. rms (injected CH)}}$$

Typical C: -120dB

Example of CH63 injection

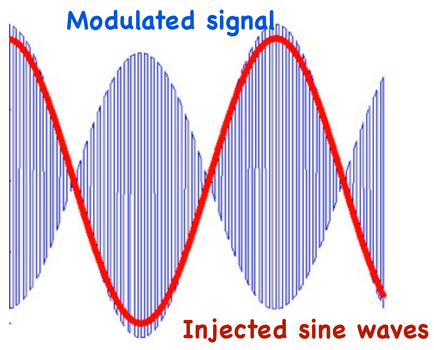


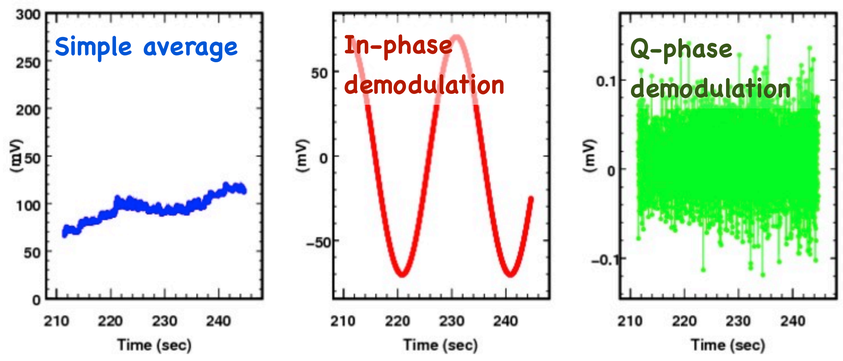
On-board demodulation

Artificial modulated signal

since waves x 4kHz square waves

→ **Successfully on-board demodulation**





Summary

Development of the ADC system for the QUIET-II experiment.

Prototype tests: The ADC board overcomes all requirements.

Next step: Synchronous run using several ADC boards and the clock master.

KEK and FNAL are using the ADC board for the new polarimeter tests.